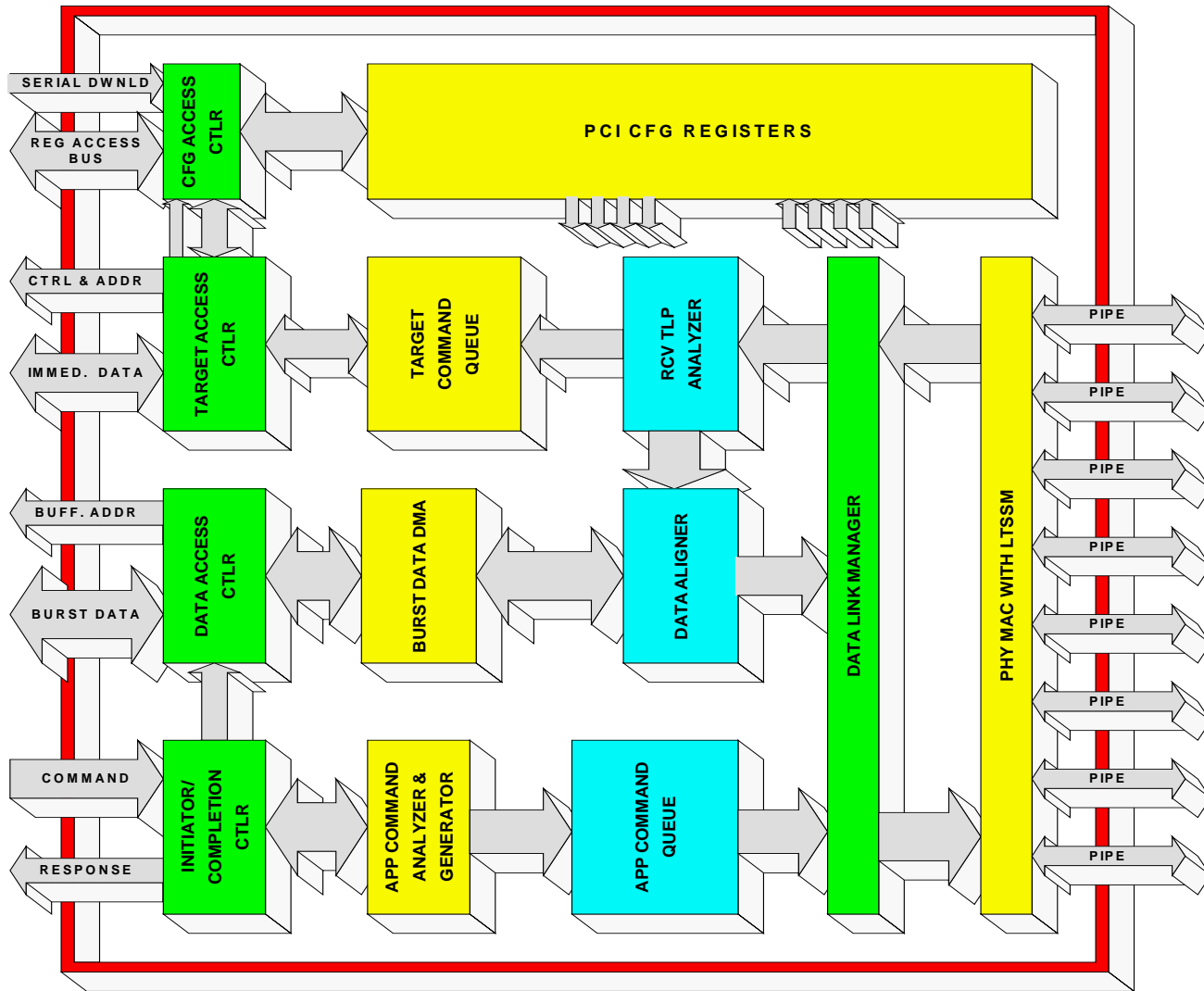


PCI-XP Controller

Highlights

- Application in End Points or Root Complex
- Configurable Design Core
- Simple Application read/write interface
- Separate Application Command, Data and Target bus
- Data bus width: 32/64/128 bit
- Complete Application isolation from PCI-Express protocol
- Support for 8 or 16 bit PIPE interface for SerDes
- Link width: 1x, 2x, 4x and 8x
- TC/VC support
- Data Alignment
- Target Receive Buffer Management
- Hardwired link Flow control

Block Diagram



Application Bus

- Buses on application side
 - Application Initiator/Completer Command Bus
 - Application Initiator/Completer data read/write bus
 - Application Target Command and data read/write bus
 - Application Reg access bus for configuration registers
 - Optional parity protection on all application buses
 - Side band signal for Messaging
 - Legacy INTx, Power Mgmt
 - Side band signal for MSI
- Serial ROM loadable or hard configurable PCI-XP configuration field options
- Software Programmable PCI-XP configuration field options
- Application bus runs at separate frequency than link frequency
- CRS (Completer Retry Status) Generation

Application Interface Highlights

- Application Interface is designed as
 - Simple command and read/write data bus
 - Complete isolation from PCI-Express issues, for example:
 - # of lanes in the link, lane reversal
 - Restriction on Max_Payload size
 - Restriction on Max_Read_Length
 - Link level flow control
 - Retry & Time out
 - Link failure and re-training
 - PCI-Express Tagging mechanism
 - DL layer TLP Frame sequencing

Application Bus Highlights

- Application Command Bus
 - Required if Application Initiator is supported
 - Fixed width
 - Side-band signal
 - Generate MSI
 - Generate Legacy Interrupt Message
- Application Data Bus
 - Required if Application Initiator is supported
 - Required if Application Target with Burstability is supported
- Application Target Bus
 - Required if Application Target is supported
 - Separate non-burstable data bus
 - Provides individual chip select for all configured BARs for a hit
 - Interrupt signal output for Root-complex support

Application Command Analyzer

- Receives and analyzes Application Initiator Command
- Maximum allowed data request length = 1KWord
- Generates of multiple command
 - As initiator for:
 - Requested Burst length exceeding Max_payload size for Mem Wr
 - Requested Burst length exceeding Max_Read_request size for Mem Rd
 - Requested Burst length+Address crosses 4KB boundary
 - As completer for:
 - Requested length exceeds Max_payload size
- Manages Command queue and provides Command Queue Status

Application Command Analyzer

- Manipulates following fields for initiator commands:
 - Data length (for division into multiple commands)
 - TC input
 - For default TC0/VC0
 - Error generation for disabled TC in VC0 Resource Control Reg
 - Address field manipulation if multiple commands are generated
- Two stage response to Application:
 - Acceptance of Command into command queue
 - Status of command with application tag
 - Data transmitted on the link for Posted Commands (DL level ACK etc)
 - Non-Posted Command Response (Cpl, CpID reception)
- Interacts with Rcv TLP Analyzer for generation of Cpl, CpID command for Application Target

Rcv TLP Analyzer

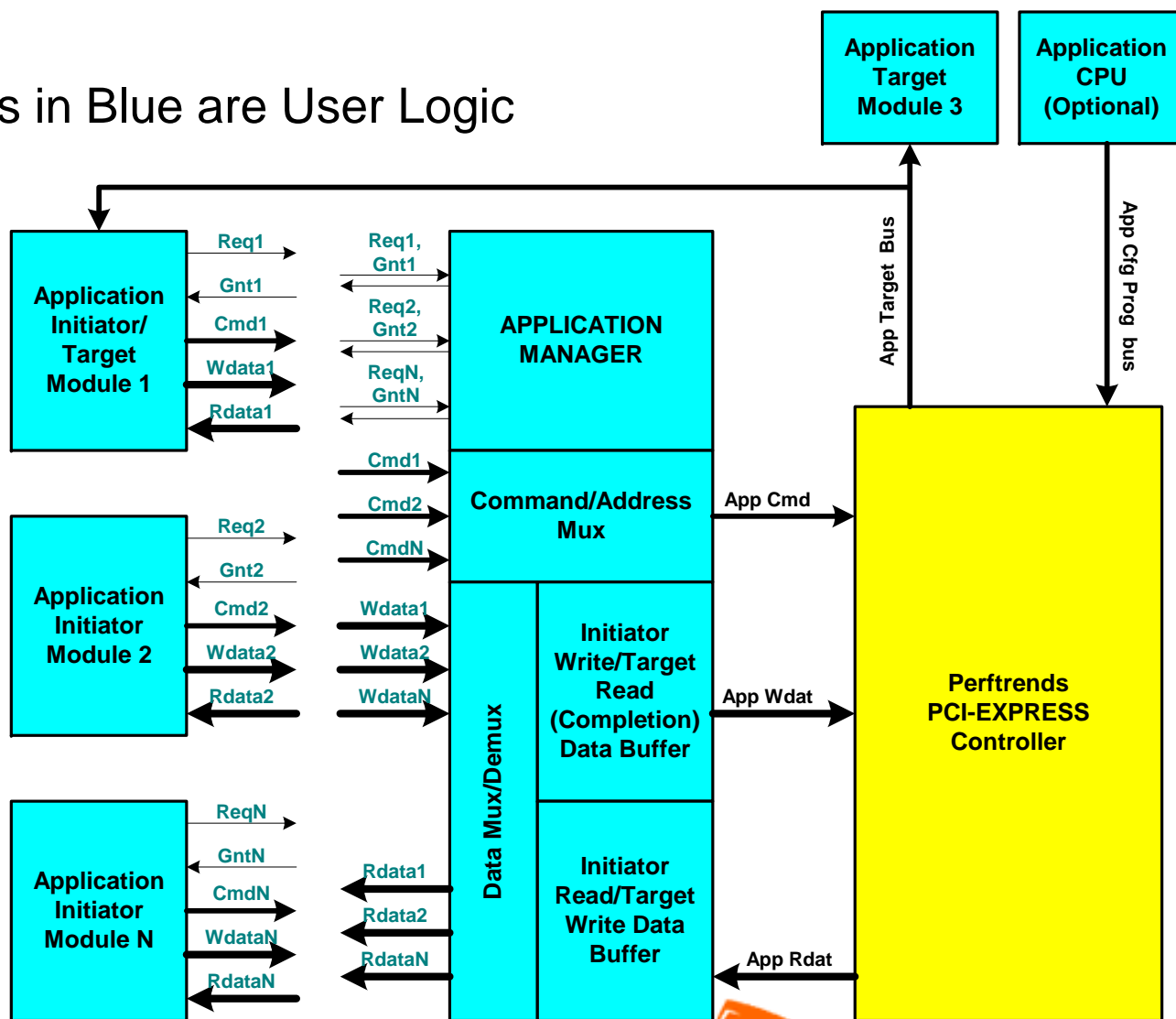
- Analyzes TLP header received in the Target Command Queue
 - For received 'cpl' or 'cpld':
 - Interacts with Application Command Analyzer for validity
 - Retrieves Application Tag from App Command Analyzer for 'cpld' to do Data DMA to Application Data Buffer
 - Provides completion status to App Command Analyzer
 - For Target Command:
 - Save command in Target Command Queue
 - Check BAR hit on all enabled functions
 - Access to PCIcfg module
 - Run bus cycle on Application Target Bus
 - Interact with App Command Analyzer for 'cpl' and 'cpld' generation
 - Generates UR or CA under certain conditions

Application Data Buffer

- Initiator Write/Completer Read Data Buffer
 - Required if Initiator Mem write data length of >2 dw supported
 - Required if Burstable Target of >2 dw supported
 - Buffer Management is in Application Layer
- Initiator Read/Target Write Data Buffer
 - Required if Initiator Mem read data length of >2 dw supported
 - Required if Burstable Target of >2 dw supported
 - Buffer Management by the Controller Rcv TLP Analyzer

Designing-In

- Blocks in Blue are User Logic



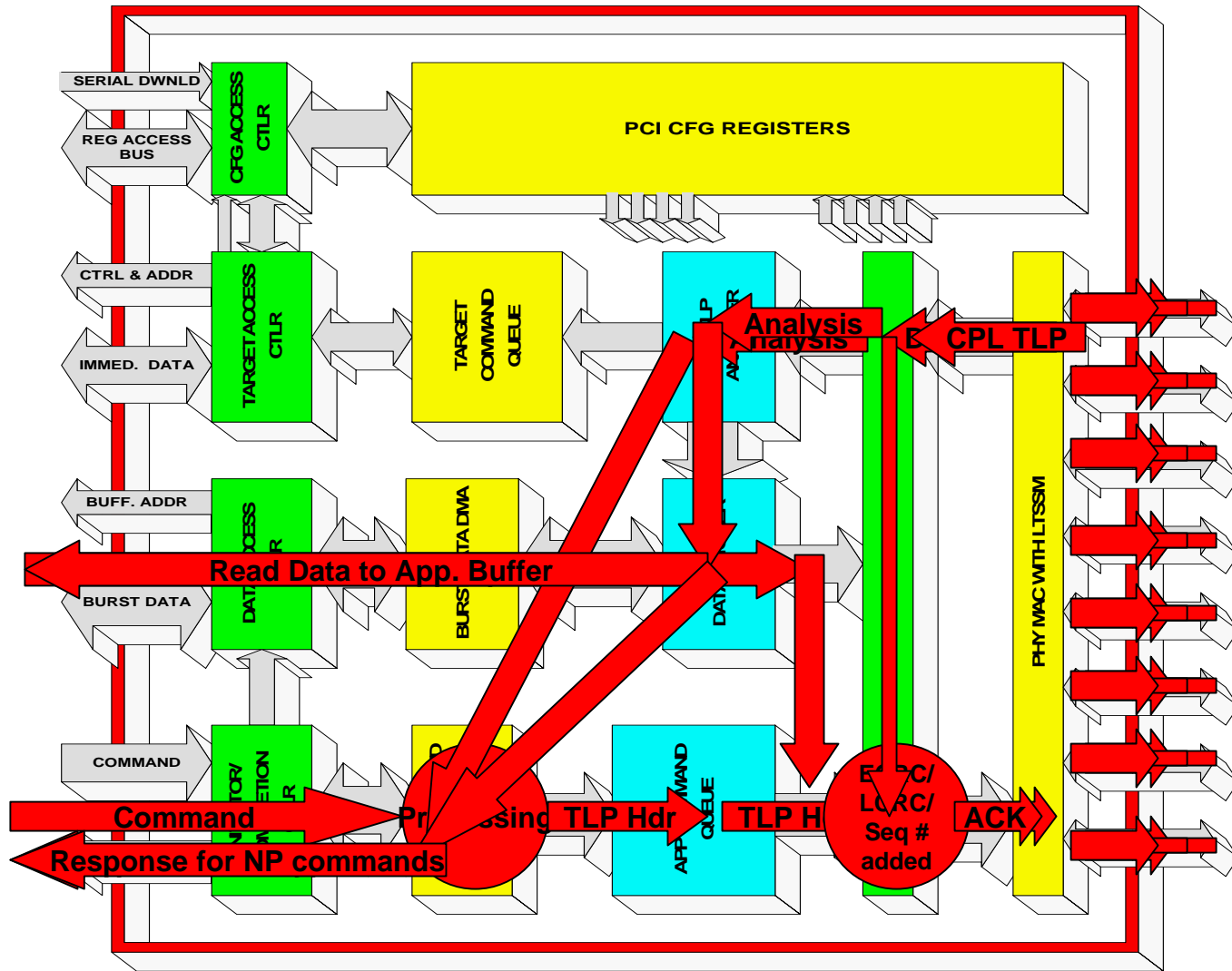
Design Core Configurability

- Maximum Link Width: 1x, 2x, 4x, 8x
- PIPE Interface width: 8/16 bit
- Application Data Bus Width: 32/64/128 bit (has relation to Link width)
- Design Core Application:
 - Root Complex
 - End Point
 - Initiator only (Burstable/Non-burstable)
 - Target only (Burstable/Non-burstable)
 - Initiator and Target (Burstable/Non-burstable)
- Depth of Initiator and Target Command Queue
- Single or Multi-function
- Configuration space
 - Hard coded or Serial ROM downloadable
- Base Address Registers
 - Number, type, size
- And many more

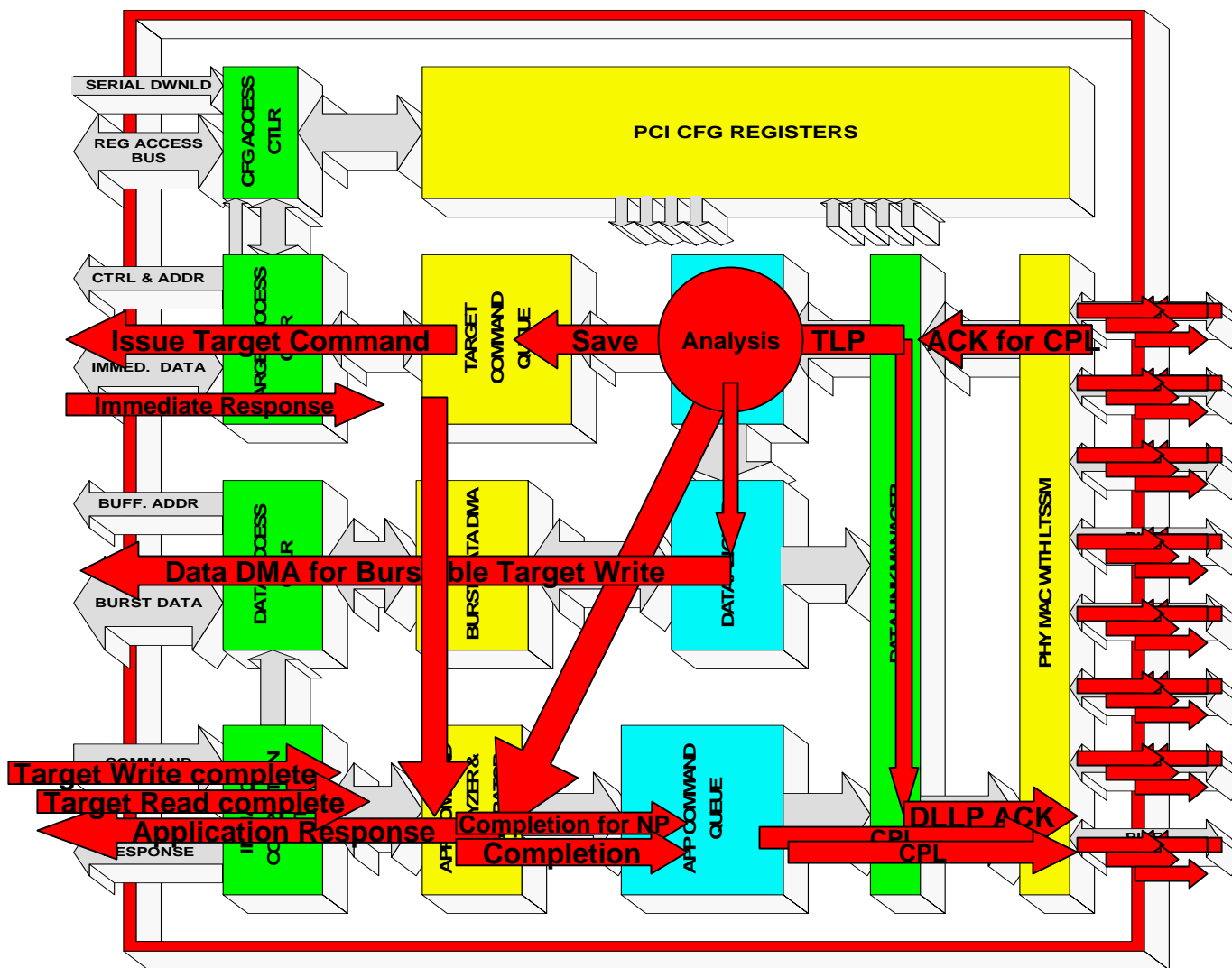
Application Programmability

- Base Address Register size
- Device ID, Vendor ID, Subsystem ID, Subsystem Vendor ID
- Posted vs Non-Posted Command Threshold as Target
- CRS (Configuration Retry Status) Disable
- All bits of Configuration Registers

Initiator Access Example



Target Access Example



Complete Feature List

- Application
 - End point
 - Root complex
- Design Core configurability
 - Simple non-burstable Initiator only
 - Simple non-burstable Target only
 - Simple non-burstable Initiator/Target
 - Burstable Initiator only
 - Burst/non-burstable Target only
 - Burstable Initiator/Target
- Simple read/write interface
 - Complete isolation of PCI-Express protocol from application
 - Traffic Class awareness if necessary
 - Burstable

Complete Feature List

- Separate Application busses
 - Command bus
 - Data bus (configurable width of 32, 64 or 128 bit)
 - Target access bus
 - PCI Cfg register access bus
 - Optional parity protection
- Highlights
 - Initiator and Target Command queue with configurable depth of up to 256 commands
 - Receive Data buffer management
 - Support for Multi-function device
 - Default TC0/VC0 and VC capability
 - Fully automatized Link flow control
 - Data assembly for receiving multiple completion
 - Automatic command segmentation for request data length more than configured max size

Complete Feature List

- Simple accept/error/retry response to the application
- Programmable Out-of-order response or In-order response
- Transaction ordering
- Automatic completion generation for non-burstable Target
- Optional End-to-end CRC (ECRC)
- Data alignment
- Data streaming
- Interrupt signal to cause MSI or Legacy Interrupt Message
- As Root Complex, MSI decode for interrupt
- Phy Interface
 - 8 or 16 bit PIPE interface
 - x8, x4, x2 and x1 link width
 - Lane reversal
 - Polarity reversal
 - LTSSM
 - Scrambler