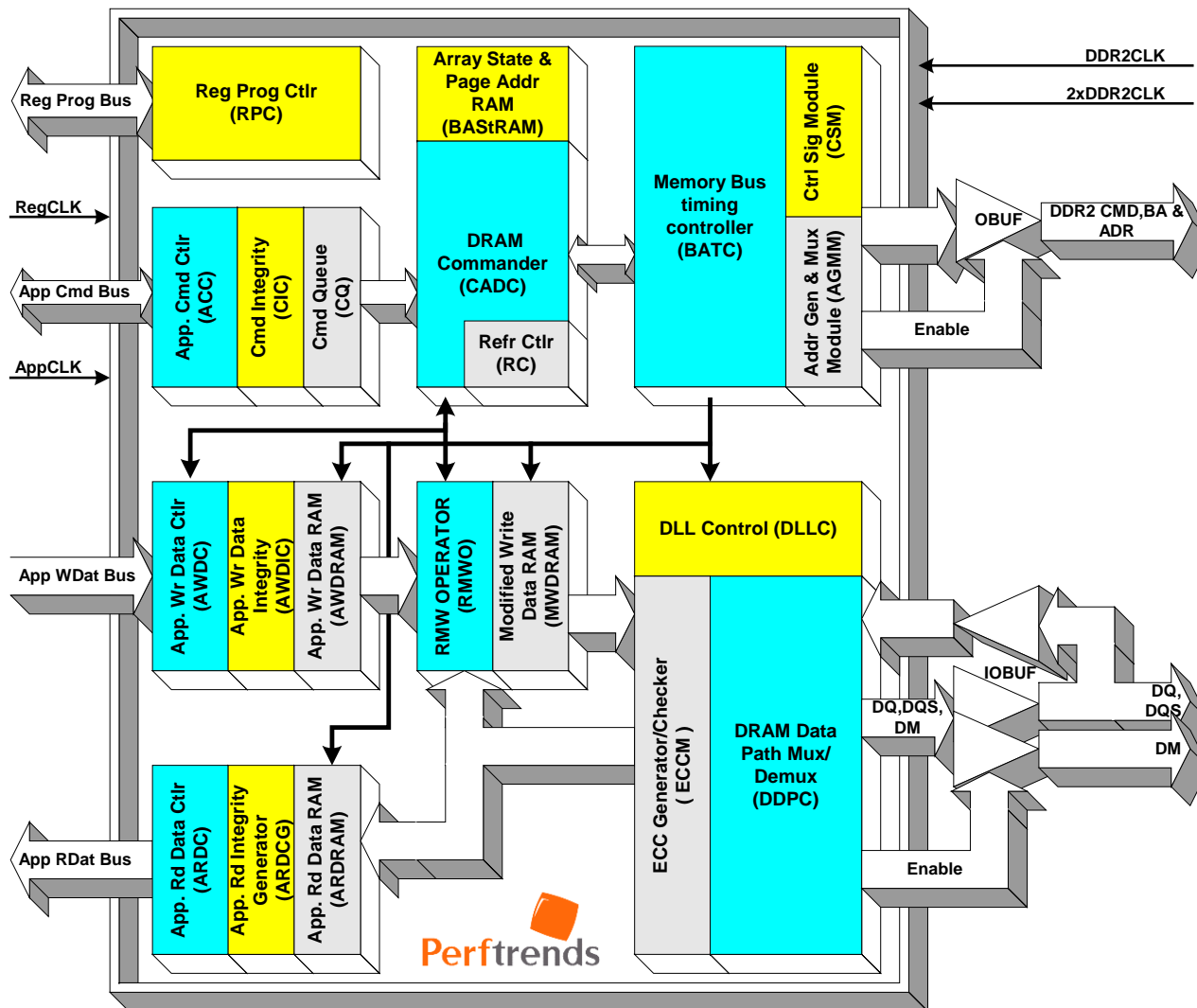


DDR2 Memory Controller

Highlights

- Low latency and high bandwidth Memory Controller
- Simple read/write Application interface
- Application bus parity protection
- PCI-Express like addressing mechanism
- Configurable Command Queue
- Up to 4KB of request data length
- Supports up to 8 separate physical memory banks
- Configurable from 16 bit to 256 bit wide Memory bus
- ECC protection
- Self-refresh hook for battery back up application
- 256 Mb to 8 Gb Memory technology
- Self-adjusting DLL for data capture
- Programmable memory timing parameters
- Programmable access behavior control
- Fast Memory Fill operation

Block Diagram

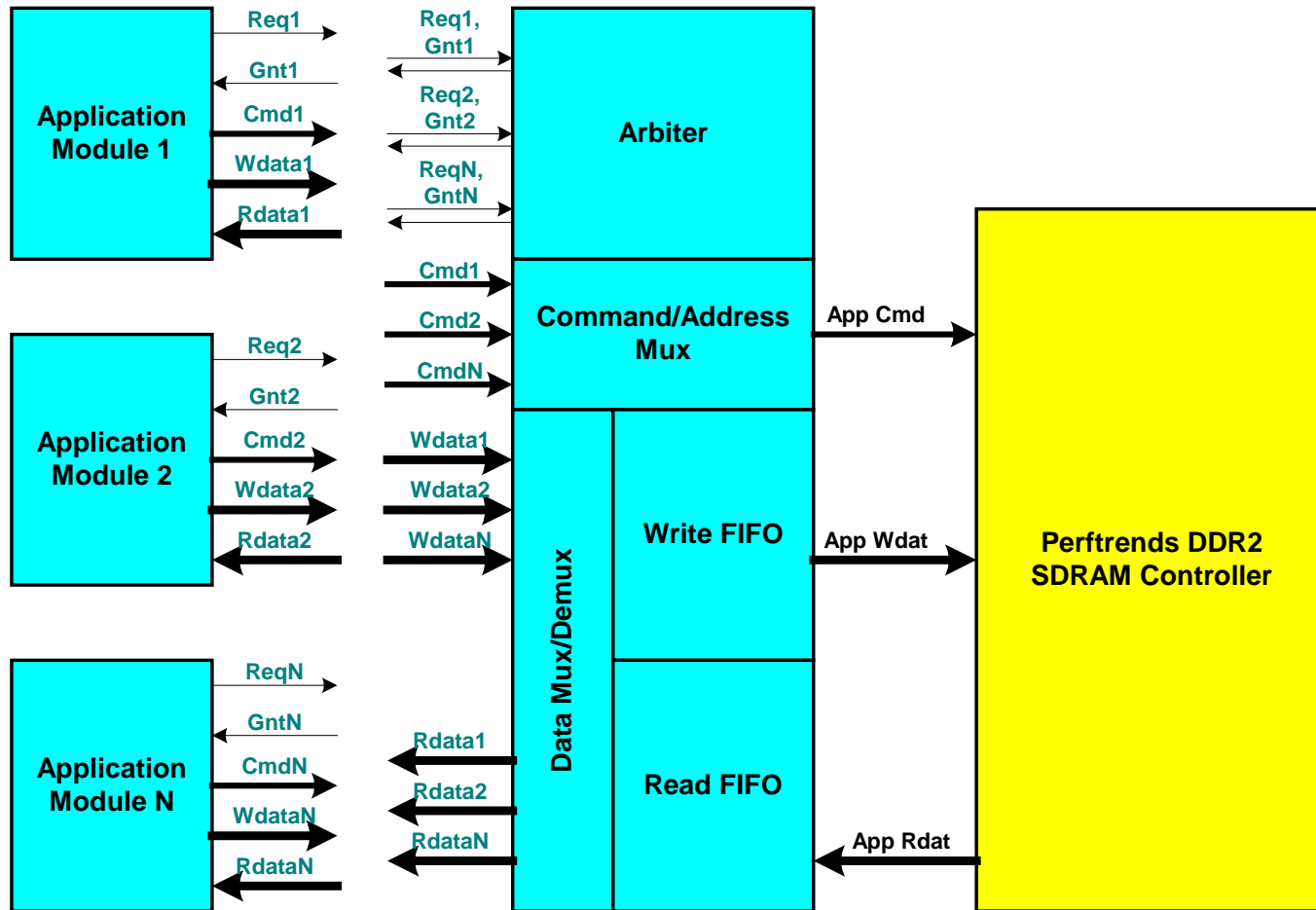


Application Bus

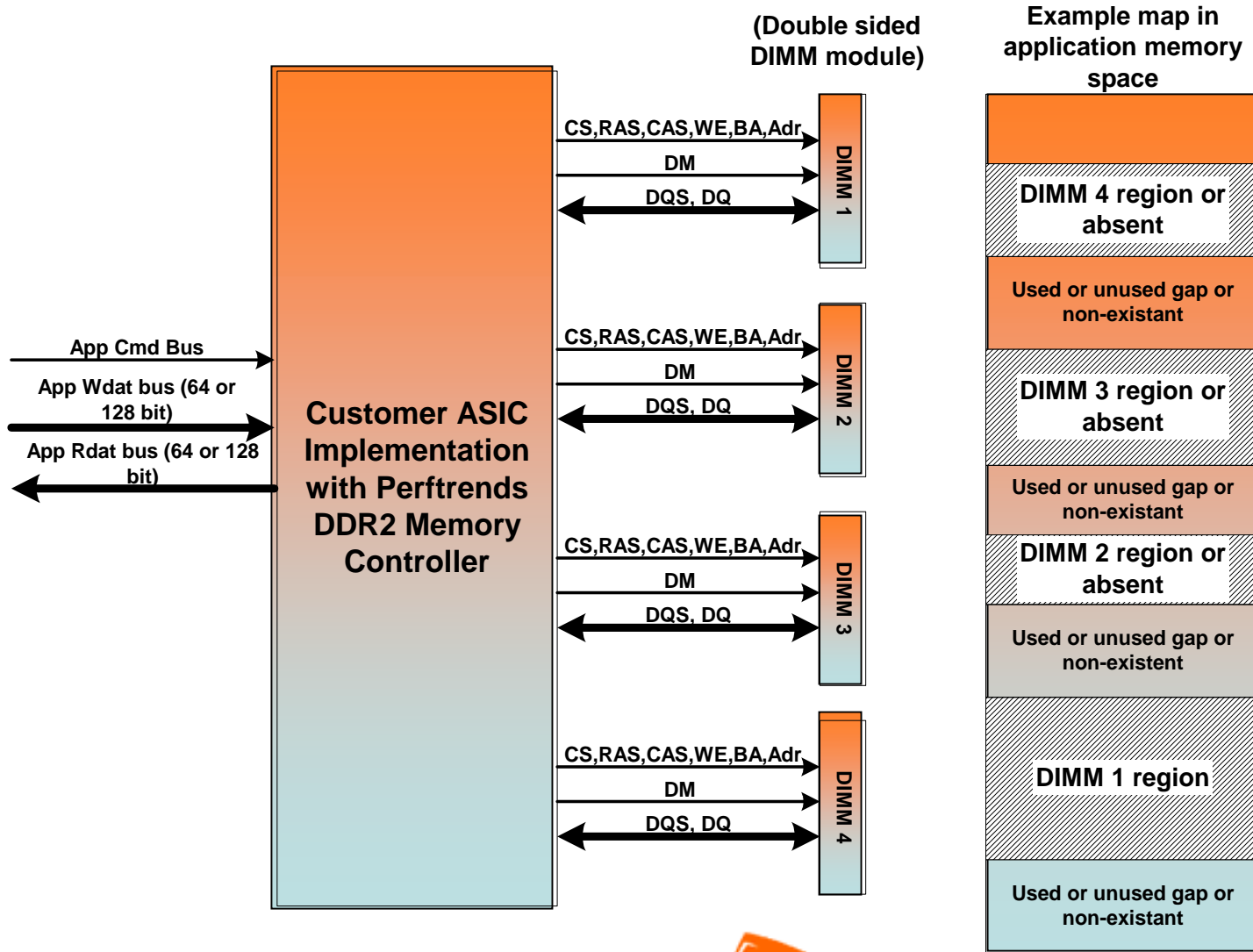
- Application Command Bus
 - Uses PCI-Express like addressing:
 - D-word address, Start byte and End byte enable
 - D-word count
- Application Read Data Bus and Write Data Bus
 - Configurable bus width based on Memory bus width (same or twice)
 - Assumes presence of Data FIFO
 - Controller writes data of received read commands in order through RDat bus
 - Controller reads data of received write commands in order through WDat bus
- Application clock can be independent of Memory clock
- Reg. Program Bus for Register Programming

Designing-In

- Application Logic in Blue



Application Example



Design Core Configurability

- Configurability is available through Perftrends Perfector program
- Configurability options are:
 - Memory Bus width
 - # of physical memory bank pairs
 - Memory ECC coverage
 - Application Data Bus width
 - Same as Memory Bus width
 - 2x Memory Bus width
 - Application bus parity coverage
 - Command Queue depth
 - And many more....

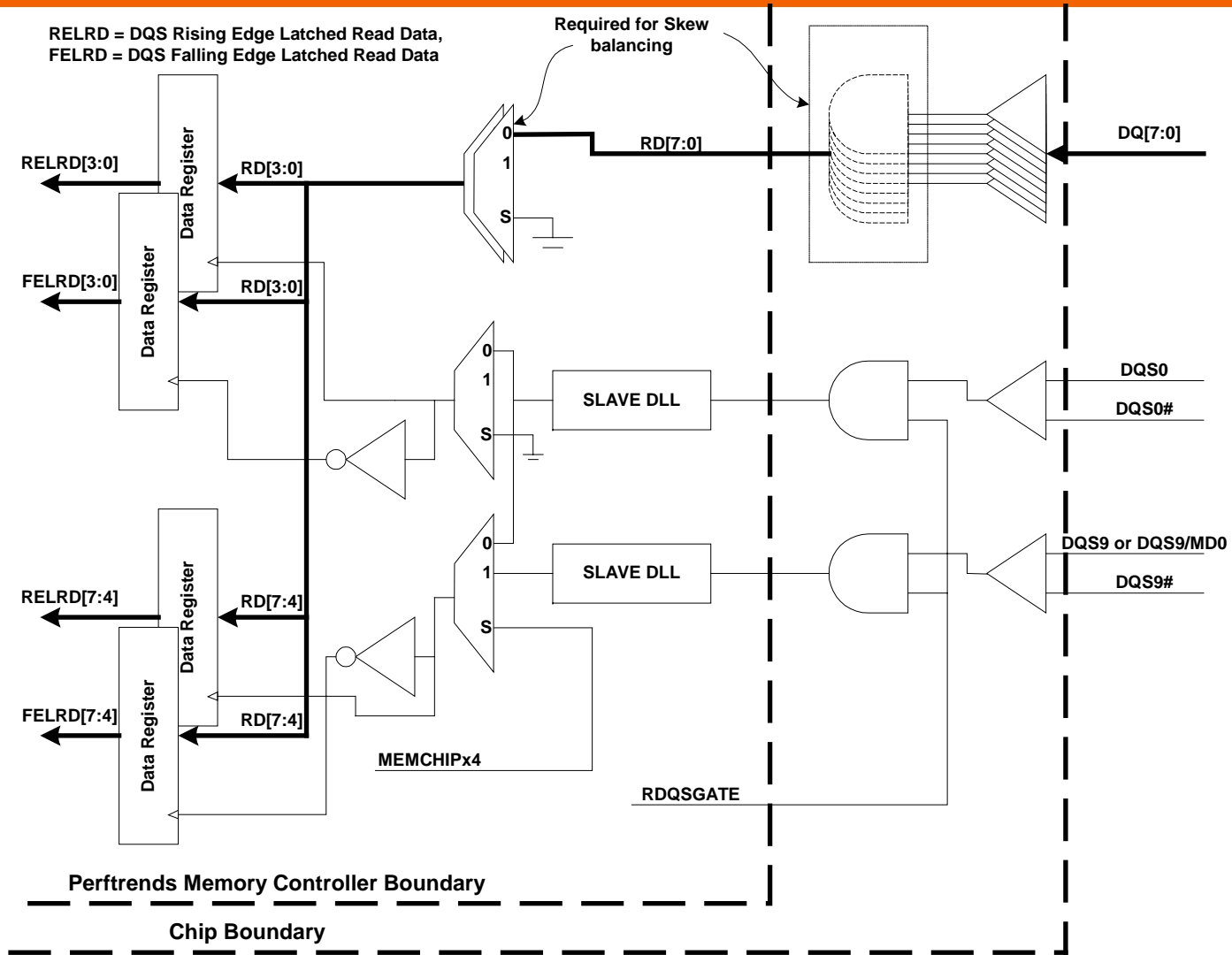
Programmable Parameters

- Memory Burst Length
- Row size, Column size, Bank Array size
- Address selection option on row, column, bank array and side
- Support for x4 type Memory (apart from x8 and x16)
- Registered or Unbuffered DIMM
- Memory timing
 - Active to Command Delay ($t_{ACD} = t_{RCD} - AL$)
 - Write Recovery Time (t_{WR})
 - Row Precharge Time (t_{RP})
 - Row Active Time (t_{RAS})
 - Read to Precharge Time (t_{RTP})
 - Additive Latency (AL)
 - Write to Read Delay (t_{WTR})
 - Row to Row Delay (t_{RRD})
- Refresh period and Refresh staggering
- ECC Enable
- And many others....

ECC (Error Correcting Code)

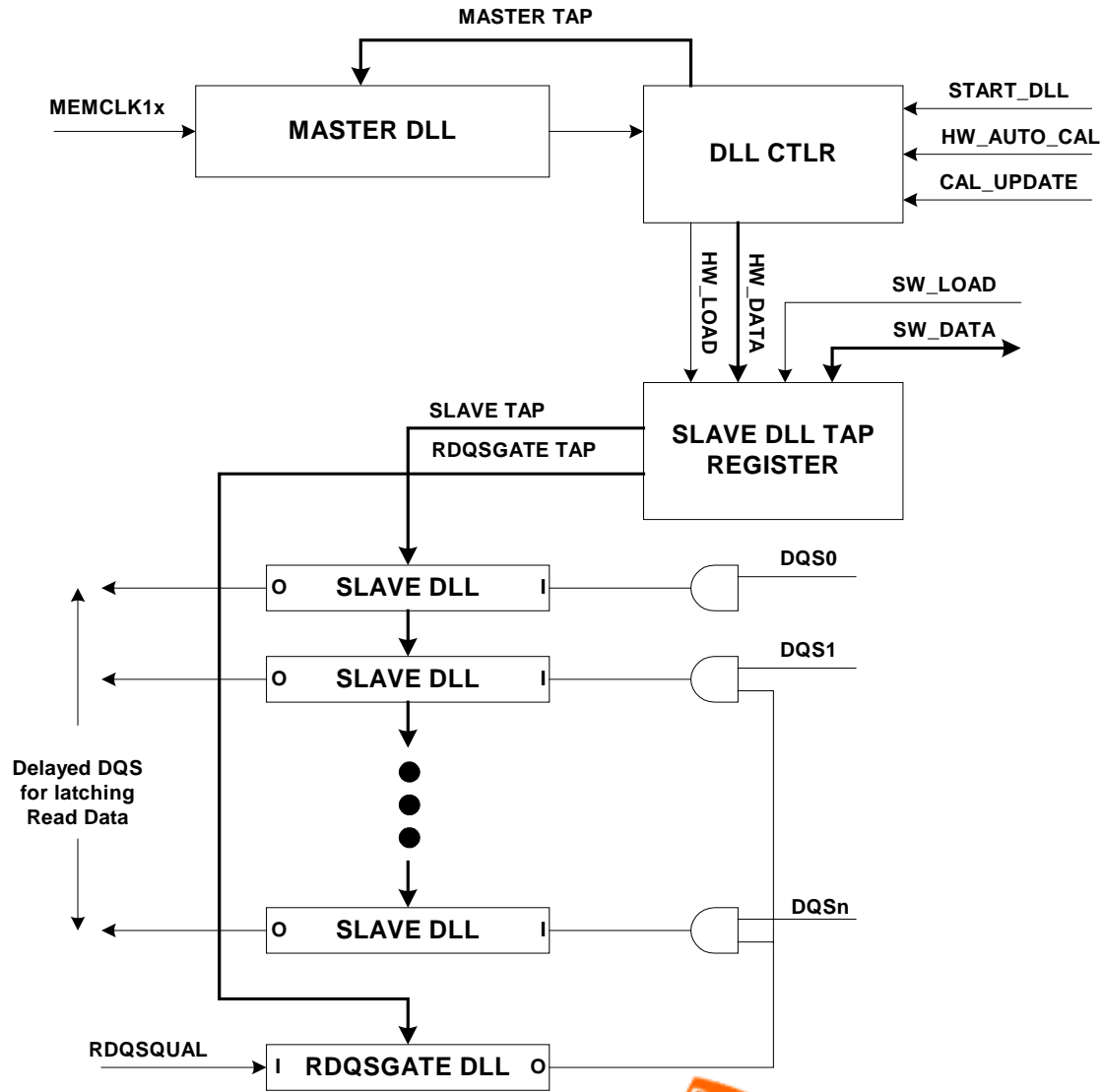
- ECC is on 64-bit data basis
- ECC is an optional feature which can be enabled or disabled
- Read Request
 - ECC is checked for single/double/multi bit failure
 - Single bit error corrected “on-the-fly” in the read data path
 - Optional feeding of all data bits ‘1’ for double/multi bit failure
 - Error type, bit position and address log
- Write Request
 - R-M-W operation for data block size < Mem bus width
 - Write only operation for data block size multiple of Mem bus width
 - Option to correct single bit error on the unmodified bytes

DLL & Read Data Path



Read Data Path with support of x4 Memory

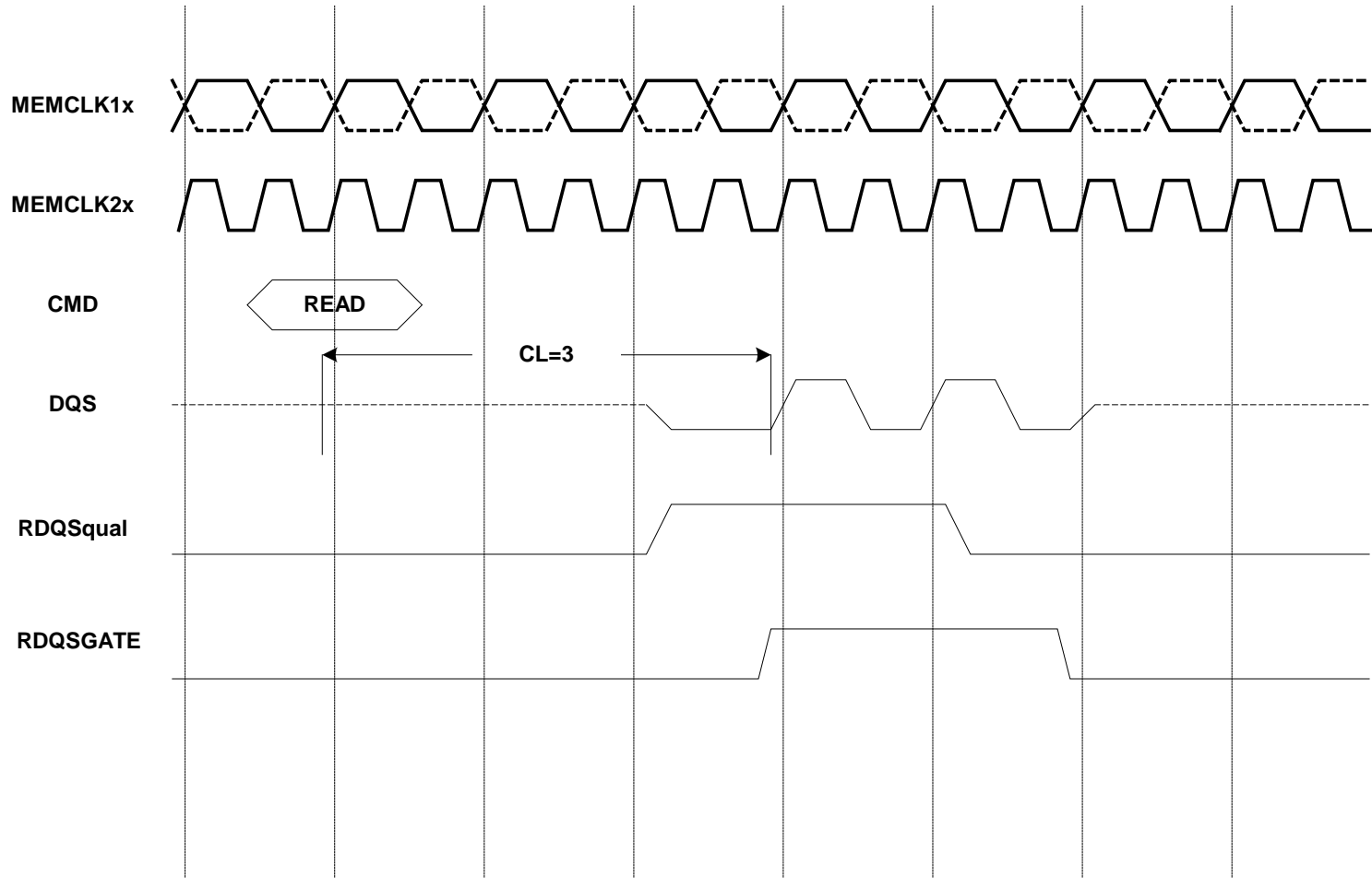
DLL



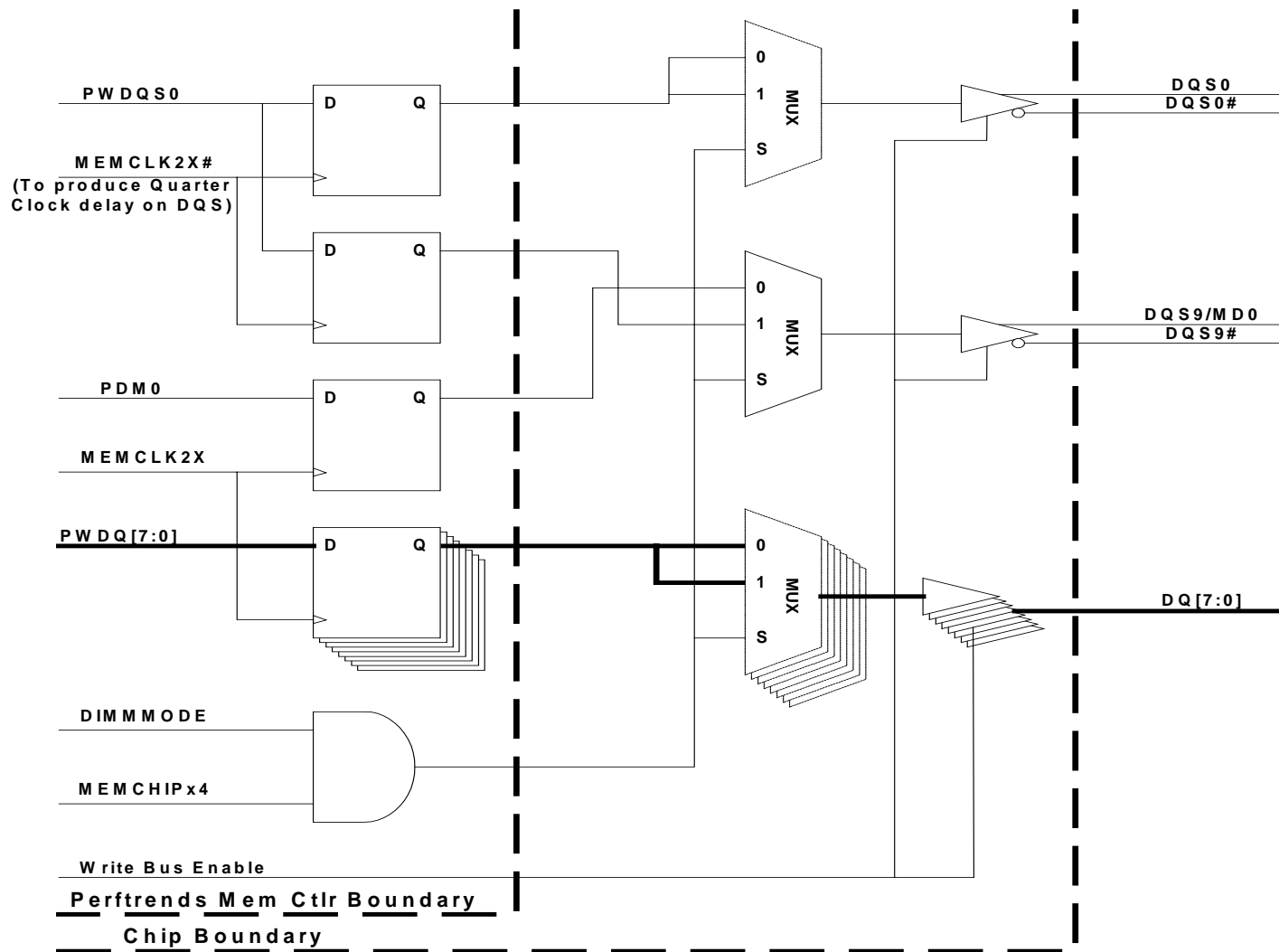
DLL

- Master DLL
 - START_DLL signal to start DLL lock operation
 - AUTO Calibration enable
 - Periodic calibration with every periodic refresh request
- Slave DLL
 - Used to delay DQS inputs in the middle of Data Valid window for read data latching
 - Hardware loadable tap at $\frac{1}{4}$ of Master tap value
 - Software programmable for any tap value
 - Auto Periodic calibration
- RDQSGATE (DQS Qualifier) DLL
 - Used for DQS input qualification to eliminate unwanted glitches
 - Tap is at $\frac{3}{4}$ of Master tap value

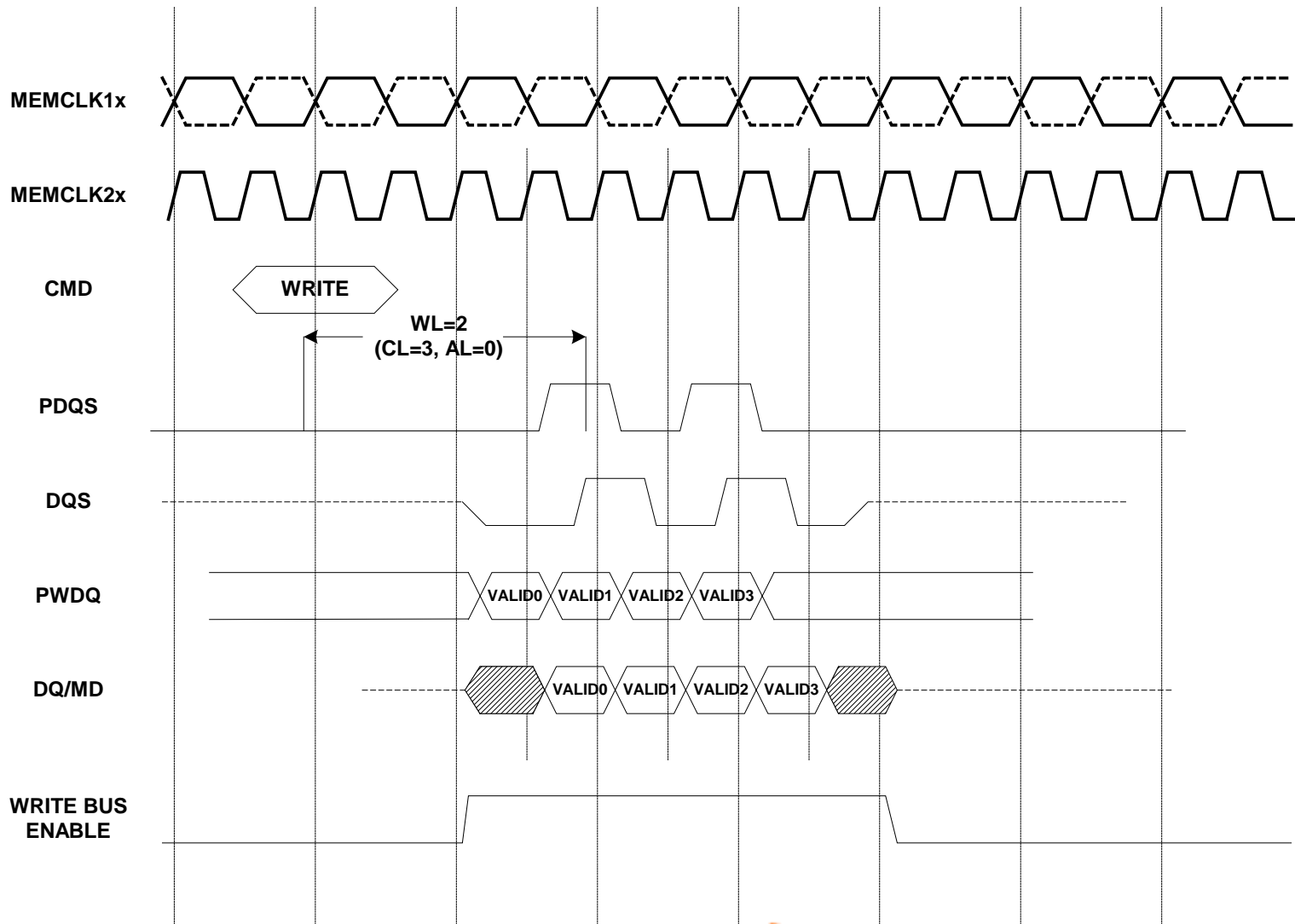
DLL: RDQSGATE timing Diagram



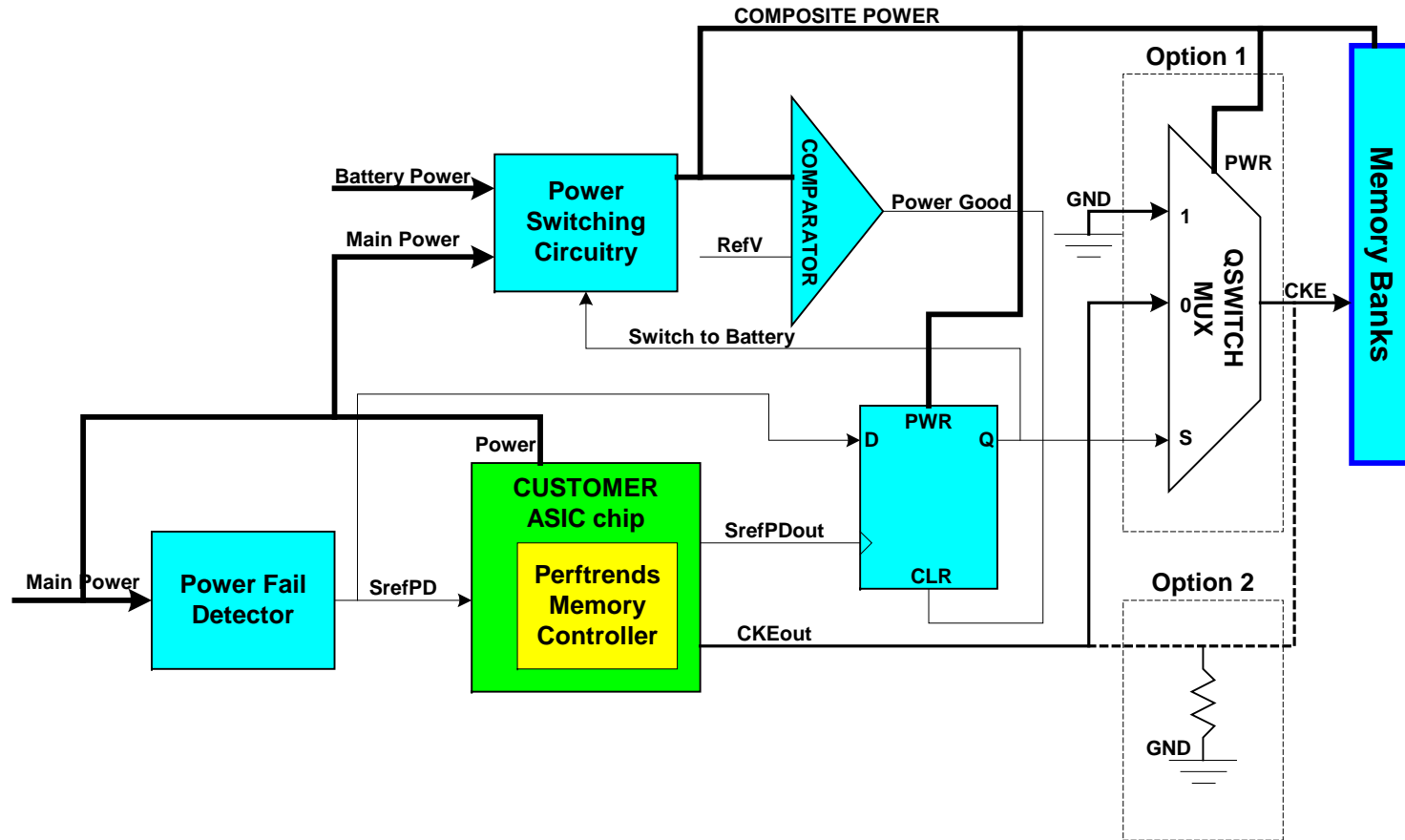
Write Data Path



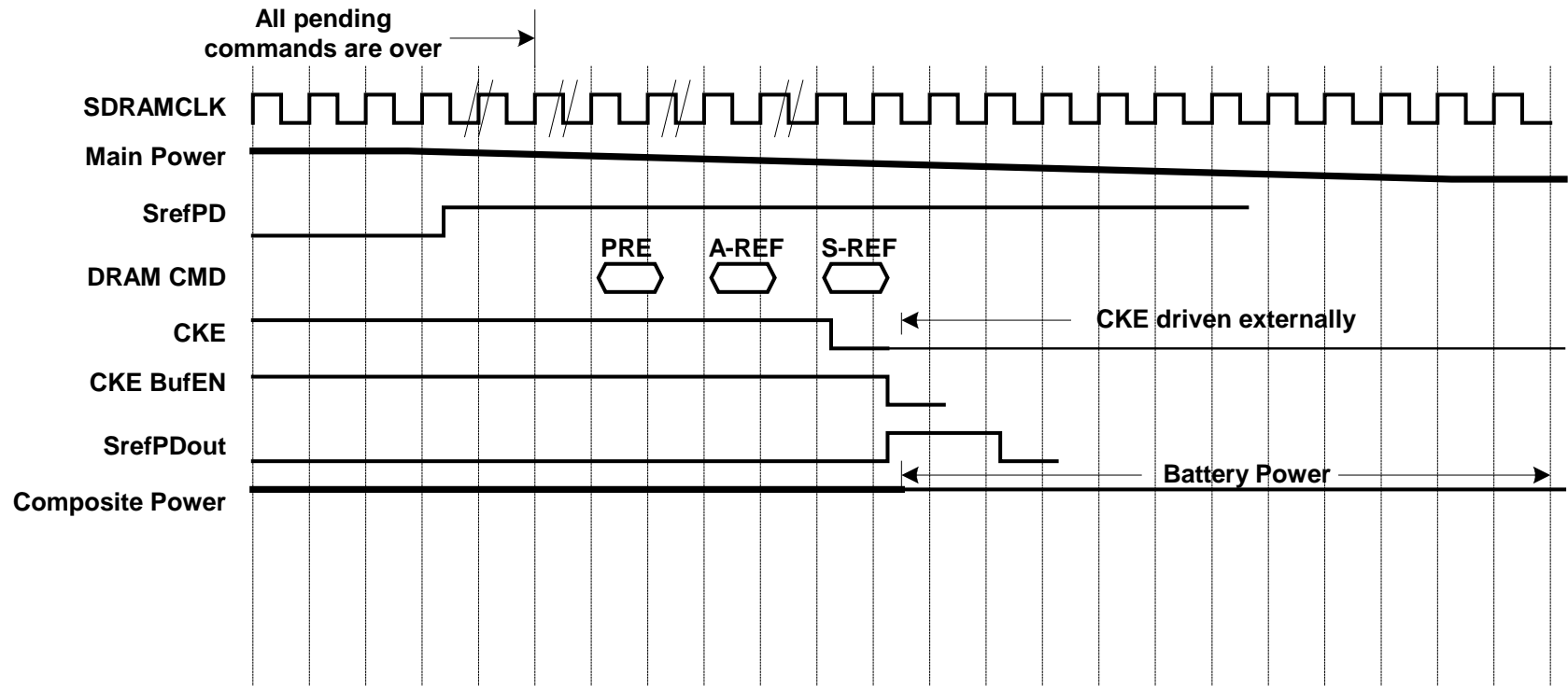
Write Data Path timing



Self Ref. & Battery Back-Up(BBU)



Self Ref. & BBU Timing



Initialization Commands

- Memory Command Register (MCR) to help setting up DRAM.
- Available commands & Usefulness:

Command	Usefulness
Mode Registers Programming	Programming any DRAM mode registers
Precharge	Precharging a physical memory bank
Refresh	Auto-refreshing a physical memory bank
Activate CKE	Activating all or a physical memory bank
Deactivate CKE with/no Self Ref.	Deactivating a physical memory bank
Memory Fill	Fast filling of physical memory bank